In the Claims:

Please amend the claims as follows:

1. (Currently amended) An overvoltage protection circuit, comprising:

a pass transistor having first and second current carrying terminals electrically connected to an input signal line and an output signal line, respectively; and

a voltage clamping circuit comprising first and second diodes electrically connected in antiparallel between a power supply line and a gate of said pass transistor, said voltage clamping circuit being sufficiently small and said pass transistor being sufficiently large that a total capacitance loading the gate of said pass transistor is less than two times a gate-to-channel capacitance of said pass transistor.

2. (Original) The circuit of Claim 1, wherein said first and second diodes comprise first and second NMOS transistors, respectively.

3. (Original) The circuit of Claim 2, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and the power supply line.

4. (Currently amended) An overvoltage protection circuit, comprising:

a pass transistor having first and second current carrying terminals electrically connected to an input signal line and an output signal line, respectively; and

a voltage clamping circuit that is electrically connected to a power supply line and a gate of said pass transistor and is configured to dynamically clamp a capacitively bootstrapped variable voltage at the gate of said pass transistor within a first range so that magnitudes of all gate-to-source, gate-to-drain and drain-to-source voltages across said pass transistor do not exceed a voltage in excess of about Vdd when Vin is equal to about 2Vdd, where Vin equals a voltage of an input signal applied to the input signal line and Vdd equals a power supply voltage on the power supply line, said voltage clamping circuit being sufficiently small and said pass transistor being sufficiently large that a total capacitance loading the gate of said pass transistor is less than two times a gate-to-channel capacitance of said pass transistor.

5. (Previously presented) The circuit of Claim 4, wherein said voltage clamping circuit comprises a plurality of transistors; and wherein said voltage clamping circuit is configured to dynamically clamp a capacitively bootstrapped voltage at a gate of said pass transistor to within a first range so that magnitudes of all gate-to-source, gate-to-drain and drain-to-source voltages across said pass transistor and all the transistors within said voltage clamping circuit do not exceed a voltage in excess of about Vdd when Vin is equal to about 2Vdd.

6. (Original) The circuit of Claim 4, wherein said voltage clamping circuit comprises an NMOS transistor that is connected as a diode between a power supply voltage and the gate of said pass transistor; and wherein a maximum voltage within the first range is equal to about Vdd+Vth, where Vth equals a threshold voltage of said NMOS transistor.

7. (Original) The circuit of Claim 4, wherein said voltage clamping circuit comprises first and second diodes electrically connected in antiparallel between the power supply line and the gate of said pass transistor.

8. (Original) The circuit of Claim 7, wherein said first and second diodes comprise first and second NMOS transistors, respectively.

9. (Original) The circuit of Claim 8, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and the power supply line.

10. (Original) The circuit of Claim 9, wherein said voltage clamping circuit and said pass transistor collectively drive the output signal line with an output signal having maximum positive voltage equal to about Vdd for Vin greater than Vdd.

11. (Previously presented) The circuit of Claim 9, wherein said voltage clamping circuit and said pass transistor are configured to collectively drive the output signal line with an output signal having a voltage that swings from a logic 0 reference level to a maximum positive voltage equal to about Vdd when Vin is switched from the logic 0 reference level to a positive voltage in a range between about Vdd and 2Vdd.

12. (Original) The circuit of Claim 10, wherein a minimum voltage within the first range is equal to about Vdd-Vth1, where Vth1 equals a threshold voltage of the first NMOS transistor.

13. (Currently amended) An overvoltage protection circuit, comprising:

first and second pass transistors of same conductivity type electrically connected in parallel between an input signal line and an output signal line;

a first power supply line electrically coupled to a gate of said second pass transistor and configured to receive a first power supply voltage;

a second power supply line configured to receive a second power supply voltage; and

a voltage clamping circuit comprising first and second diodes electrically connected in antiparallel between said second power supply line and a gate of said first pass transistor; and

wherein a threshold voltage of said second pass transistor and the first power supply voltage are at values that cause said second pass transistor to turn on before said first pass transistor when the input signal line is switched high-to-low relative to the first power supply voltage.

14. (Currently amended) The circuit of Claim 13, wherein said first and second diodes comprise first and second NMOS transistors, respectively; and wherein each of said first and second NMOS transistors is smaller than said first pass transistor.

15. (Original) The circuit of Claim 14, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said first pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and said second power supply line.

16. (Previously presented) The circuit of Claim 14, wherein said voltage clamping circuit is configured to clamp the gate of said first pass transistor at a maximum voltage of about $Vdd2+V_{TN2}$ in response to a positive input voltage transition in excess of about $V_{TN1}+V_{TN2}$ on the input signal line, where V_{TN1} and V_{TN2} are the threshold voltages of the first and second NMOS transistors, respectively.

17. (Previously presented) The circuit of Claim 16, wherein said voltage clamping circuit is configured to clamp a voltage at the gate of said first pass transistor at a minimum voltage of about $Vdd2-V_{TN1}$ in response to application of a logic 0 signal to the input signal line, where V_{TN1} is a threshold voltage of the first NMOS transistor.

18. (Original) The circuit of Claim 16, wherein said first and second pass transistors comprise third and fourth NMOS transistors, respectively; and wherein V_{TN2} is about equal to a threshold voltage of the third NMOS transistor.

19. (Original) The circuit of Claim 13, wherein said first and second power supply lines are electrically connected together.

20. (Currently amended) An overvoltage protection circuit, comprising:

a first pass transistor having a first current carrying terminal electrically connected to an input signal line and a second current carrying terminal electrically connected to an output signal line; **[[and]]**

a voltage clamping circuit that is electrically connected to a gate electrode of said first pass transistor and is configured to clamp a bootstrapped voltage at the gate electrode to a first voltage below a maximum voltage on the input signal line upon completion of a pull-up interval and is further configured to clamp the bootstrapped voltage at the gate electrode to a second voltage that is unequal to the first voltage and higher than a minimum voltage on the input signal line upon completion of a pull-down interval; and

a second pass transistor of same conductivity type as said first pass transistor and having a first current carrying terminal electrically connected to the input signal line, a second current carrying terminal electrically connected to the output signal line and a gate terminal that is held at a fixed voltage, said second pass transistor having a threshold voltage set at a value that causes said second pass transistor to turn on before said first pass transistor turns on when the input signal line switches high-to-low relative to the fixed voltage.

21. (Original) The circuit of Claim 20, wherein the first voltage is greater than the second voltage.

22. (Original) The circuit of Claim 21, wherein said voltage clamping circuit comprises first and second diodes electrically connected in antiparallel between a power supply line and the gate electrode.